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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
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Subject: Serial No. 09/498,739 02/07/00

Chiun-Chi Shen

A DELAY LOCKING HIGH SPEED CLOCK SYNCHRONIZATION METHOD AND CIRCUIT

Grp. Art Unit: 2824

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

Saeki et al., "A 2.5-ns Clock Access, 250-MHz, 246-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid State Circuits, Vol. 31 No. 11, Nov. 1996, pp. 1656-1664, describes the structure and timing of the clock distribution within the SDRAM.

Yamada et al., "Capacitance coupled Bus with Negative Delay Circuit for High speed and Low Power (10GB/s<500mW) Synchronous DRAMs", Digest of Papers for IEEE Symposium on VLSI Circuits, 1996, pp. 112-113, describes a mirror control circuit MCC which is a latch that fixes the delay segment of the forward delay element FDA selected to be transferred to the backward delay array BDA.

U.S. Patent 5,742,194 to Saeki, "Internal Clock Generator for a Synchronous Dynamic RAM", describes an internal clock generator for a SDRAM.

U.S. Patent 5,410,263 to Waizman, "Delay Line for On-Chip Clock Synthesis with Zero Skew and 50% Duty Cycle", teaches an integrated circuit for synthesizing a 50% duty cycle internal clock that is synchronized with zero pulse difference with respect to an external reference clock having a frequency that is equal to, or is a sub-multiple of the synthesized internal Clock.

U.S. Patent 5,923,613 to Tien et al., "Latched Type Clock Synchronizer with Additional 180 Degrees Phase Shift Clock", describes a multiple phase latched type synchronized clock circuit.

Sincerely,

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